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June 5, 2002

VIA FACSIMILE

To: Examiner Erik Kielin
Group Art Unit No. 2813
U.S.P.T.O.

Facsimile No.: (703) ~~306-7722~~ 305-1341

From: Sean M. McGinn

Facsimile No.: (703) 761-2375

Re: Enclosed Supplemental § 1.111 Amendment
U.S. Patent Application Serial No. 09/902,483
Our Ref: YOR.129CIP

Dear Examiner Kielin:

Enclosed is a Supplemental Amendment, which should place the above-referenced case in condition for allowance.

Thank you in advance for your kind consideration on this case.

Very truly yours,

Sean M. McGinn

SMM/sm
Enclosure

Total No. of Pages Transmitted: 18

#13/ Supp Amdt B OK DN 10/10/02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Cabral et al.

Serial No.: 09/902,483 Group Art Unit: 2813

Filed: July 11, 2001 Examiner: Erik Kielin

For: SELF-ALIGNED SILICIDE (SALICIDE) PROCESS FOR LOW RESISTIVITY CONTACTS TO THIN FILM SILICON-ON-INSULATOR AND BULK MOSFETS AND FOR SHALLOW JUNCTIONS

Honorable Assistant Commissioner of Patents
Washington, D.C. 20231

SUPPLEMENTAL AMENDMENT UNDER 37 C.F.R. §1.111

Sir:

Further to the Amendment filed May 14, 2002, please amend the above- identified application as follows:

IN THE CLAIMS:

Sub C1 B4

1. (Amended) A method for fabricating a silicide for a semiconductor device, said method comprising:

depositing a metal containing silicon or an alloy thereof on a silicon substrate;

reacting said metal containing silicon or said alloy to form a first silicide phase;

etching any unreacted metal containing silicon or alloy;

depositing a silicon cap layer over said first silicide phase;

reacting the silicon cap layer to form a second silicide phase, for said semiconductor device; and

etching any unreacted silicon from said silicon cap layer.